Claims:

1. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a resist over a crystal semiconductor comprising a part to become a channel forming region;

forming a dotted hole in said resist by patterning said resist using electron drawing method or FIB method;

forming a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region, the step of forming said plurality of impurity regions being conducted by introducing a first impurity thereinto through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween.

2. A method as claimed in claim 1 further comprising the steps of:

forming a gate insulating film over said part to become the channel forming region after the step of forming said plurality of impurity regions; and

forming a gate electrode over said part to become the channel forming region with said gate insulating film therebetween.

3. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region.

4. A method as claimed in claim 3 wherein said heat treatment is conducted at a temperature of 1000 to 1200 °C.

5. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon and containing boron to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide and to make said boron segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region.

6. A method as claimed in claim 5 wherein said heat treatment is conducted at a temperature of 1000 to 1200 °C.

7. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

implanting an oxygen ion into a crystal semiconductor comprising a part to become a channel forming region by a convergent ion beam or an electron beam, said crystal semiconductor comprising silicon;

thermally treating said crystal semiconductor comprising silicon to change a region thereof implanted with said oxygen ion by said implanting step into an oxide region which forms a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region; and

introducing into said crystal semiconductor an impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween.

8. A method as claimed in claim 7 further comprising the steps of:

forming a gate insulating film over said part to become the channel forming region after the thermally treating step; and

forming a gate electrode over said part to become the channel forming region with said gate insulating film therebetween.

9. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

introducing a first impurity into a crystal semiconductor having a part to become a channel forming region to form a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region, said plurality of impurity regions containing an element selected from the group consisting of carbon, nitrogen and oxygen as said first impurity; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween.

10. A method as claimed in claim 9 further comprising the steps of:

forming a gate insulating film over said part to become the channel forming region after the step of introducing the first impurity; and

forming a gate electrode over said part to become the channel forming region with said gate insulating film therebetween.

11. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region, and

wherein said impurity is added by said adding step to said substrate to a depth deeper than an etched depth formed in said groove-like or hole-like pattern by said anisotropic etching.

12. A method as claimed in claim 11 wherein said heat treatment is conducted at a temperature of 1000 to 1200 °C.

13. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

introducing a first impurity into a crystal semiconductor having a part to become a channel forming region to form a plurality of impurity regions which form a dotted pattern in said part to become a channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region, said plurality of impurity regions containing an element selected from the group consisting of carbon, nitrogen and oxygen as said first impurity;

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said channel forming region includes intervals, and said impurity regions alternates with said intervals in a direction of a channel width W of said channel forming region, and

wherein said impurity regions have total width of Wpi in a direction of said channel width W, and a total of said intervals is Wpa in said direction of said channel width W, where Wpi/W = 0.1 to 0.9 and Wpa/W = 0.1 to 0.9.

14. A method as claimed in claim 13 further comprising the steps of:

forming a gate insulating film over said part to become the channel forming region after the step of introducing the first impurity; and

forming a gate electrode over said part to become the channel forming region with said gate insulating film therebetween.

15. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a resist over a crystal semiconductor comprising a part to become a channel forming region;

forming a dotted hole in said resist by patterning said resist using electron drawing method or FIB method;

forming a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region, the step of forming said plurality of impurity regions being conducted by introducing a first impurity thereinto through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said dotted pattern has an arrangement in which said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

16. A method as claimed in claim 15 further comprising the steps of:

forming a gate insulating film over said part to become the channel forming region after the step of forming said plurality of impurity regions; and

forming a gate electrode over said part to become the channel forming region with said gate insulating film therebetween.

17. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region, and

wherein said dotted pattern has an arrangement in which said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

18. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming a gate insulating film and a gate electrode on said channel forming region; and

in said channel forming region, forming a region in which carriers move, and impurity regions which pin a depletion layer that expands from said drain region toward said channel forming region and said source region, artificially and locally.

19. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming a gate insulating film and a gate electrode on said channel forming region; and

in said channel forming region, forming a region in which carriers move, and impurity regions which control the threshold voltage to a predetermined value voltage by the addition of impurity elements, artificially and locally.

20. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming impurity regions artificially and locally in said channel forming region; and

forming a gate insulating film and a gate electrode on said channel forming region,

wherein impurity elements that expand an energy band width (Eg) are artificially and locally added to said impurity regions.

21. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming a gate insulating film and a gate electrode on said channel forming region; and

in order to form impurity regions which pin a depletion layer that expands from said drain region toward said channel forming region and said source region, artificially and locally adding impurity elements that expand an energy band width (Eg) to said channel forming region.

22. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming a gate insulating film and a gate electrode on said channel forming region; and

in order to form impurity regions which control the threshold voltage to a predetermined value voltage by addition of impurity elements, artificially and locally adding impurity elements that expand an energy band width (Eg) to said channel forming region.

23. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

forming a source region, a drain region and a channel forming region using a crystal semiconductor; and

artificially and locally forming impurity regions by addition of impurity elements that expand an energy band width (Eg) in said channel forming region; and

forming a gate insulating film and a gate electrode formed on said channel forming region,

wherein said impurity regions have an insulating property, and

wherein said impurity elements are not added or are added by a very small amount in a region other than said impurity regions in said channel forming region.

24. A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein a region other than said impurity region within said channel forming region is intrinsic or substantially intrinsic region.

25. A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

26. A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an

assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

27. A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

28. A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein said crystal semiconductor is a monocrystal semiconductor.

29. A method of manufacturing an insulated gate semiconductor device as claimed in claim 18, wherein said impurity regions are in a dot pattern.

30. A method as claimed in claim 19, wherein a region other than said impurity regions within said channel forming region is an intrinsic or substantially intrinsic region.

31. A method as claimed in claim 19, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

32. A method as claimed in claim 19, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an

assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

33. A method as claimed in claim 19, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

34. A method as claimed in claim 19, wherein said crystal semiconductor is a monocrystal semiconductor.

35. A method as claimed in claim 19, wherein said impurity regions are in a dot pattern.

36. A method as claimed in claim 19, wherein said impurity elements are one or a plurality of kinds of elements selected from carbon, nitrogen and oxygen.

37. A method as claimed in claim 20, wherein a region other than said impurity regions within said channel forming region is an intrinsic or substantially intrinsic region.

38. A method as claimed in claim 20, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of $Wpi/W = 0.1$ to 0.9, $Wpa/W = 0.1$ to 0.9 and $Wpi/Wpa = 1/9$ to 9 are accomplished between W, Wpi and Wpa.

39. A method as claimed in claim 20, wherein at least one section perpendicular to a channel direction of said

channel forming region is substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

40. A method as claimed in claim 20, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

41. A method as claimed in claim 20, wherein said crystal semiconductor is a monocrystal semiconductor.

42. A method as claimed in claim 20, wherein said impurity regions are in a dot pattern.

43. A method as claimed in claim 20, wherein said impurity elements are one or a plurality of kinds of elements selected from carbon, nitrogen and oxygen.

44. A method as claimed in claim 21, wherein a region other than said impurity regions within said channel forming region is an intrinsic or substantially intrinsic region.

45. A method as claimed in claim 21, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

46. A method as claimed in claim 21, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

47. A method as claimed in claim 21, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

48. A method as claimed in claim 21, wherein said crystal semiconductor is a monocrystal semiconductor.

49. A method as claimed in claim 21, wherein said impurity regions are in a dot pattern.

50. A method as claimed in claim 21, wherein said impurity elements are one or a plurality of kinds of elements selected from carbon, nitrogen and oxygen.

51. A method as claimed in claim 22, wherein a region other than said impurity regions within said channel forming region is an intrinsic or substantially intrinsic region.

52. A method as claimed in claim 22, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

53. A method as claimed in claim 22, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

54. A method as claimed in claim 22, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

55. A method as claimed in claim 22, wherein said crystal semiconductor is a monocrystal semiconductor.

56. A method as claimed in claim 22, wherein said impurity regions are in a dot pattern.

57. A method as claimed in claim 22, wherein said impurity elements are one or a plurality of kinds of elements selected from carbon, nitrogen and oxygen.

58. A method as claimed in claim 23, wherein a region other than said impurity regions within said channel forming region is an intrinsic or substantially intrinsic region.

59. A method as claimed in claim 23, wherein assuming that a width of said channel forming region is W, a total width of said impurity regions is Wpi, and a total of intervals of said impurity regions is Wpa, respectively, relational expressions of Wpi/W = 0.1 to 0.9, Wpa/W = 0.1 to 0.9 and Wpi/Wpa = 1/9 to 9 are accomplished between W, Wpi and Wpa.

60. A method as claimed in claim 23, wherein at least one section perpendicular to a channel direction of said channel forming region is substantially regarded as an assembly of a plurality of channel forming regions which are sectioned by said impurity regions.

61. A method as claimed in claim 23, wherein said impurity regions are arranged at intervals of 100 to 3000 Å.

62. A method as claimed in claim 23, wherein said crystal semiconductor is a monocrystal semiconductor.

63. A method as claimed in claim 23, wherein said impurity regions are in a dot pattern.

64. A method as claimed in claim 23, wherein said impurity elements are one or a plurality of kinds of elements selected from carbon, nitrogen and oxygen.

65. A method as claimed in claim 17 wherein said heat treatment is conducted at a temperature of 1000 to 1200 °C.

66. A method of manufacturing an insulated gate semiconductor device, said method comprising the steps of:

locally conducting an anisotropic etching on a surface of a substrate comprising silicon and containing boron to draw a groove-like or hole-like pattern in a part of said substrate to become a channel forming region;

adding said surface of said substrate with an impurity selected from the group consisting of carbon, nitrogen and oxygen;

embedding said groove-like or hole-like pattern with thermal oxide by conducting a heat treatment on said substrate after the adding step to make said impurity segregated in said thermal oxide and to make said boron segregated in said thermal oxide,

wherein said impurity segregated in said thermal oxide forms a plurality of impurity regions which form a dotted pattern in said part to become the channel forming region as viewed from above said part to become the channel forming region toward a direction of depth of said channel forming region,

wherein said dotted pattern has an arrangement in which said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region.

67. A method as claimed in claim 66 wherein said heat treatment is conducted at a temperature of 1000 to 1200 °C.